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The Intermediate Silicon Layers (ISL) detector is presently being built as part of CDF upgrades. The ISL is a large radius (28 cm) silicon tracker with a total active area of about 3.5 m^2. The challenge is to build a device which provides precise 3D points introducing a minimal amount of material for the supporting structure. The design and the status of the project are described.

1. INTRODUCTION

The Tevatron $p\overline{p}$ Collider and the CDF detector are presently being upgraded for Run II operation (to begin in early 2000). The Tevatron center-of-mass energy will be increased from 1.8 TeV to 2.0 TeV and the instantaneous luminosity by almost one order of magnitude, to reach 1-2$\times 10^{32}$ cm^{-2} sec^{-2}. The bunch spacing will be reduced from 3.7 μs, first to 396 ns and then, during the second part of the Run, to 132 ns. The CDF goal for Run II is to take 2 fb^{-1} of data [1].

CDF will have two mechanically separate silicon detectors: the Silicon Vertex (SVX II)[2] and the Intermediate Silicon Layers detector (ISL), both using double-sided sensors. SVX II has five layers located between the minimum distance of $\sim$2.5 cm and the maximum distance of $\sim$10.6 cm from the beamline. With a total length of $\sim$1 m, it covers the pseudorapidity region $|\eta|<2$. The ISL is located between SVX II and the Central

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Outer Tracker (COT), with one central layer (6 C) at ∼23 cm from the beamline and two forward/backward layers (6 and 7 F/B) respectively at ∼20 and ∼29 cm from the beamline. Layer 6C covers the region $|\eta|<1$, while layers 6 and 7 F/B cover the region $1<|\eta|<2$. The total length of the detector is ∼2 m (Fig. 1).

The measurement of 5+1 3D points matched to the COT information provides a robust tracking in the central region. In the forward region, where the acceptance of the COT rapidly decreases, silicon-only tracking will be done using the measurement of 5+2 3D points. Simulations show that the silicon-only tracker has $\sigma_{p_t} \sim 0.4\ \%/p_t^2$. The ISL increases the efficiency and the purity of single and double b tagging in the forward region and its fine granularity helps to resolve tracking ambiguities within stiff jets, often produced in $t\bar{t}$ events.

The ISL is a challenging project: ∼900 large area double-sided silicon detectors will be mounted on 296 ladders, for a total of ∼3.5 m^2 total active area (∼300,000 channels). The design for the support structure (spaceframe) foresees a system of hollow carbon fiber flanges connected by hollow carbon fiber rods. Carbon fiber was chosen to minimize material and maximize rigidity. The readout electronics and DAQ already designed for the SVX II will be used. The readout will operate in deadtimeless mode at the rate of 50 MHz. The cooling system has to dissipate ∼1.2 kW produced by the readout electronics.

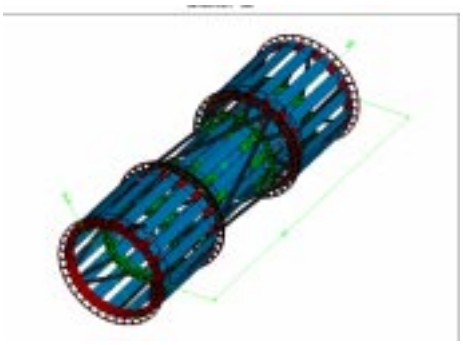

Figure 1. The ISL detector. The four flanges 7 and one every other module are drawn. In the lower part some rods connecting the two external flanges 6 and 7 can be recognised. In the central part layer 6 C modules are visible.

2. ISL COMPONENTS

The ISL ladder is made of three silicon detectors bonded together to form one single electrical unit and glued on a carbon fiber support. The readout hybrid is mounted off silicon and glued on the edge of the support. Two ladders butted head to head form the modules (∼55 cm long) mounted on the spaceframe.

2.1. Silicon detectors

The ISL uses double-sided AC coupled microstrip detectors made from high resistivity n-type silicon bulk material. Detectors have 512 strips/side with a pitch of 112 micron. On one side there is a stereo angle of 1.2^o. The active area is 5.7×7.5 cm^2 for layer 7 detectors, produced by Micron Semiconductors on 6" wafers[3], and 5.7×6.7 cm^2 for layer 6, produced by Hamamatsu Photonics on 4" wafers. Although more challenging, the 6" technology has the convenience of accomodating two detectors on each wafer. Both Micron and Hamamatsu detectors have polysilicon bias resistors on both sides and common p-stops on the n^+ side.

The design is to have a depletion voltage ∼40 V, with a breakdown voltage of coupling capacitors >120 V. This allows to follow the increasing of depletion voltage with radiation damage, which anyway is expected to be rather low for the ISL. Since the total ladder length is >20 cm, the interstrip capacitance/cm is kept at a level <1.0-1.2 pF/cm in order to reduce the total capacitance load to the readout chip amplifier and consequently the noise. Electrical tests show that prototypes delivered by Micron are now meeting specifications and final production has begun. The measured value of coupling capacitance (between the single strip and the backplane) is 150 pF both on the p-side and on the n-side, with a bias resistance of 4-6 MΩ and an interstrip resis-

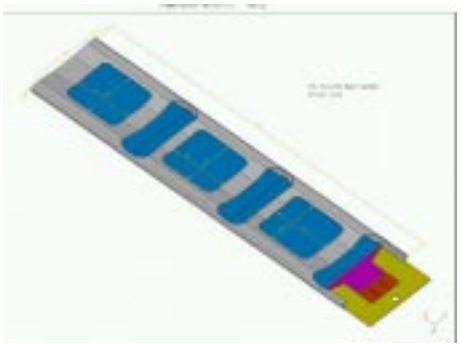

Figure 2. The ISL ladder. The holes on the body of the support are for the assembly jig towers and for the microbonding machine. The hybrid is glued and microbonded on one edge of the ladder.

tance > 2 GΩ. The level of broken capacitors and leaky strips is better than the requested 3 %.

Micron prototypes performance was also tested during 1997 testbeam at Fermilab[4]. The resolution is 25 μm, with an average signal/noise ratio of 21, measured using SVX electronics, and an average cluster size of 1.7 strips (with no magnetic field). No significant signal loss is observed as a function of incoming particle interstrip position.

2.2. Frontend electronics

Signals from the silicon detectors are read out by the SVX3 chips[5], which perform signal integration, analog pipelining to provide the delay required by Level 1 trigger latency, digital conversion, and data sparsification for each of the 128 channels per chip. The SVX3 chip continuosly performs the analog data acquisition during digitization and readout, which allows operation for Level 1 accept rates up to 50 kHz.

The ISL DAQ system is basically identical to that used for SVX II, with the only difference being the hybrid design and placement. The ISL hybrid is made of Aluminum Nitride and hosts four SVX3 chips on each side. Since the SVX3 chip has been designed to match the pitch of the SVX II detectors (60 μm), a pitch adapter is mounted on the hybrid to match the 112 μm pitch of the ISL detectors. The cables connecting the hybrids to the portcards are about 1 m long and, to avoid problems in signal amplitude and synchronization, a transceiver chip is mounted on the ISL hybrid to convert the signals to low voltage differentials. A precision hole is drilled in order to fix the hybrid to the assembly jig and give a point of reference to the Coordinate Measuring Machine. This hole is also used to fix the module to the spaceframe with a pin.

2.3. Supports and assembly procedure

The geometry and the openings made on the body of the ladder carbon fiber supports allow an easy assembly and microbonding (Fig.2). Full torsional rigidity of the ladder is reached after sensor gluing. Tests show that there is no additional noise due to the electromagnetic coupling between silicon and supports (antenna effect) in the region of gluing, where the two surfaces are separated only by $\sim$100 μm of glue[4]. To reduce any possible effect, also a layer of insulating kapton is inserted.

For assembly, the support is positioned on the Al bridge of the jig and the hybrid and the three silicon detectors are mounted on four independent rotating towers. After having aligned the detectors to the hole on the hybrid, gluing is performed. The residual interstrip misalignment has been measured to be <5 μm, with a detector aplanarity <30 μm. The bowing of the entire module is of the order of 100 μm.

3. ISL SPACEFRAME

3.1. Design

The spaceframe is made of eight hollow carbon fiber rings (flanges) connected by carbon fiber rods. It is supported and anchored to the COT endplates by two extensions fixed to the external flanges 7. The design foresees also a carbon fiber outer screen which will give an enormous rigidity to the whole structure. The ISL spaceframe will also provide support for the SVX II detector.

The lamination of the components of the flanges uses 4 layers of carbon fiber, each 125 μm thick, assembled with a stardard manual lay-up

Figure 3. The aluminum prototype of the ISL spaceframe fully assembled.

technology. This technology has the advantage of reliability and low cost. Lamination of flanges and rods production is done by two italian companies, Monfrini S.R.L. and Reglass S.p.A.

The desired precision of 50 μm in the position of the modules cannot be reached if the modules are directly fixed on the flanges, because the flanges can be positioned only with a precision of $\sim$100 μm. Instead, thin layers of beryllium (ledges) are fixed on the flange using dedicated tooling, which allows to compensate for the global misalignemnt of the flange, and the modules are then mounted on the beryllium ledges.

3.2. Aluminum prototype

A full size Aluminum prototype of the spaceframe was built in order to test the alignment and mounting procedure (Fig. 3). This prototype was also used to optimize the routing of cables connecting hybrids to the portcards, which are fixed to the ISL extension. Cables run parallel to the detector axis and to the magnetic field. This avoids possible interactions with the currents running on the cables. No residual stresses between aluminum flanges and carbon fiber rods were found after the glue had settled. This gives a reasonable confidence that no stresses will be present in the real spaceframe. Finally, this model was used to study the routing of the cooling pipes.

4. COOLING

The cooling system is challenging since it needs to remove the heat produced by the 2,400 readout chips (0.5 W/chip) and mantain the silicon below 20^o C and the hybrid below 25-30^o C. This will be done by flowing a low temperature liquid in a aluminum pipe glued to the berillium ledges which act as heat sinks. To have a low pressure and temperature drop along the pipes, the design foresees to divide each of the three(two) layer 6(7) barrels into three(four) identical sectors and to have an independent cooling circuit for each sector. Tests show that a flux of 0.6 l/m of a 30 % mixture of water and glycol at 4.5^o C keeps the desired temperature. The external diameter of pipes is 4.5 mm, which is large enough to allow an easy bending. To avoid liquid losses, the cooling liquid is maintained at a pressure below 1 atm.

5. CONCLUSION

The design and the status of the project of the CDF Intermediate Silicon Layers detector have been reviewed. R&D has been completed and production of components is beginning. The expectation is to have all the components tested during the year 1999 and the detector assembled for CDF Run II in early 2000.

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